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Address to:

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney's Docket No. NSC1-H1700
[P04797]

First Named Inventor DAVID W. CARLSON

UTILITY PATENT APPLICATION TRANSMITTAL
(under 37 CFR 1.53(b))

SIR:

Transmitted herewith for filing is the patent application entitled:

METHOD FOR PLANARIZING A THIN FILM



CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date October 2, 2000, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EL254114063US addressed to: Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

LANA T. BRENNER

(Name of person mailing paper)

(Signature)

Enclosed are:

1. Transmittal Form (two copies required)
2. The papers required for filing date under CFR § 1.53(b):
 - i. 11 Pages of specification (including claims and abstract);
 - ii. 2 Sheets of drawings.
_____ formal informal
3. Declaration or oath
 - a. Newly executed (original or copy)
4. Microfiche Computer Program (Appendix, see 37 CFR 1.96)
5. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - i. Computer Readable Copy
 - ii. Paper Copy (identical to computer copy)
 - iii. Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

6. An assignment of the invention to NATIONAL SEMICONDUCTOR CORPORATION is attached (including Form PTO-1595).
 - i. 37 CFR 3.73(b) Statement (when there is an assignee)
7. Power of Attorney
8. An Information Disclosure Statement (IDS) is enclosed, including a PTO-1449 and copies of _____ references.
9. Preliminary Amendment.
10. Return Receipt Postcard (MPEP 503 -- should be specifically itemized)
11. Other

12. FOREIGN PRIORITY

Priority of application no. filed on in is claimed under 35 USC 119.

The certified copy of the priority application:

- is filed herewith; or
- has been filed in prior application no. NEW filed on HEREWITH, or
- will be provided.

 English Translation Document (if applicable)

13. FEE CALCULATION

a. Amendment changing number of claims or deleting multiple dependencies is enclosed.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee (\$710)
Total Claims	17 - 20	* 00	x \$18.00	00
Independent Claims	1 - 3	* 00	x \$80.00	00
<u> </u> Multiple dependent claim(s), if any			\$270.00	00

*If less than zero, enter "0".

Filing Fee Calculation \$710.00

50% Filing Fee Reduction (if applicable) \$

14. Small Entity Status

- A small entity statement is enclosed.
- A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
- is no longer claimed.

15. Other Fees

Recording Assignment [\$40.00] \$40.00
 Other fees
Specify _____ \$

Total Fees Enclosed \$750.00

16. Payment of Fees

Check(s) in the amount of \$ 750.00 enclosed.
 Charge Account No. 12-1420 in the amount of \$.
A duplicate of this transmittal is attached.

17. All correspondence regarding this application should be forwarded to the undersigned attorney:

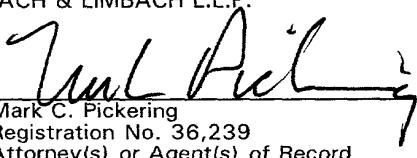
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18. Authorization to Charge Additional Fees

The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 12-1420. A duplicate of this transmittal is attached.

LIMBACH & LIMBACH L.L.P.

By:


Mark C. Pickering
Registration No. 36,239
Attorney(s) or Agent(s) of Record

October 2, 2000
(Date)

Attorney Docket No. NSC1-H1700
[P04797]

METHOD FOR
PLANARIZING A THIN FILM

BACKGROUND OF THE INVENTION

5

1. Field of the Invention.

The present invention relates to a method for chemical-mechanical polishing and, more particularly, to a method for chemical-mechanical polishing to form a thin film.

10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95
2. Description of the Related Art.

During the fabrication of many semiconductor circuits, the individual devices that make up the circuits are fabricated, in part, by forming a number of layers of material on a wafer and then selectively etching one or more of the layers of material to leave the individual devices. The result of this etch step, however, produces a severe topology with the individual devices forming high points and the etched-away portions forming low points.

FIG. 1 shows a cross-sectional diagram that illustrates a prior-art processed wafer 100 following the etch step that defines the individual devices that make up the circuits on wafer 100. As shown in FIG. 1, wafer 100 has a number of individual devices 110 and a number of etched-away portions 112. In addition, wafer 100 has a top surface 114 with high points defined by the top surfaces of the individual devices 110 and low points defined by the top surfaces of the etched-away portions 112.

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One problem with a severe topology is that it is difficult to form a thin, planarized layer of polysilicon on this type of surface. A thin, planarized layer of polysilicon can be used to implement, for example, a local interconnect line. One well-known technique for forming 5 planarized surfaces is known as chemical-mechanical polishing (CMP).

With CMP, an uneven surface is both chemically reacted and mechanically ground to bring down the surface until a substantially flat surface is formed. Conventional CMP processes, however, are subject to dishing, a term that refers to low spots in an otherwise relatively flat 10 surface.

If a layer of polysilicon is deposited on the surface of a processed wafer, such as wafer 100, using conventional deposition techniques, and then planarized using conventional CMP processes, dishing tends to remove a significant amount of polysilicon from the top edges of the 15 individual devices. FIGs. 2A and 2B shows cross-sectional diagrams that illustrate the conventional deposition of polysilicon and subsequent planarization using CMP processes.

As shown in FIG. 2A, conventional deposition techniques have been used to form a layer of polysilicon 210 on the top surface 114 of 20 wafer 100. Conventional CMP planarization requires overdepositing of the material to be planarized by 2x-3x the required final thickness. For example, oxide is typically deposited to a thickness of 12K-18K angstroms to obtain a final thickness of 6.5K angstroms.

Current-generation deposition equipment limits the maximum 25 thickness of the deposited polysilicon to approximately 5K angstroms. (Thicker layers of polysilicon produce film stresses that deform the wafer.) Thus, a final thickness of approximately 2.5K angstroms is the maximum thickness obtainable with current-generation equipment.

Next, as shown in FIG. 2B, polysilicon layer 210 is planarized using chemical-mechanical polishing (CMP) until a thin, substantially-flat layer of polysilicon remains on the surfaces of devices 110. As further shown in FIG. 2B, the CMP process tends to remove more polysilicon at 5 the edges of the top surfaces of devices 110 than at the centers.

This can lead to degraded device performance where the polysilicon has been thinned as shown by arrow A, to an outright open circuit where the polysilicon has been completely removed at the edges as shown by arrow B. Thus, there is a need for a method of forming a 10 thin, planarized layer of polysilicon on the devices which is not subject to polysilicon thinning at the edges of the top surfaces of the devices.

SUMMARY OF THE INVENTION

15 The method of the present invention substantially eliminates the dishing that occurs when polysilicon is planarized using chemical-mechanical polishing. As a result, a thin, planarized layer of polysilicon can be formed over the individual devices of a semiconductor circuit to form, for example, local interconnect lines.

20 In accordance with the present invention, the method includes the step of forming a layer of first material on the top surface of a wafer. The top surface of the wafer having a wafer lower level and a wafer upper level that lies above the wafer lower level. In addition, the top surface of the layer of first material has a first lower level and a first 25 upper level that lies above the first lower level.

The method also includes the step of forming a layer of second material on the top surface of the layer of second material. The method further includes the step of chemically-mechanically polishing the layer of second material and the underlying layer of first material until the

layer of second material is substantially, completely removed from the layer of first material to form a planarized layer of material.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed 5 description and accompanying drawings that set forth an illustrative embodiment in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

10 FIG. 1 is a cross-sectional diagram illustrating a prior-art processed wafer 100 following the etch step that defines the individual devices that make up the circuits on wafer 100.

FIGs. 2A and 2B are cross-sectional diagrams illustrating the conventional deposition of polysilicon and subsequent planarization 15 using CMP processes.

FIGs. 3A-3B are cross-sectional drawings illustrating a method for forming a thin, planarized layer of polysilicon in accordance with the present invention.

20 DETAILED DESCRIPTION

FIGs. 3A-3B show cross-sectional drawings that illustrate a method for forming a thin, planarized layer of polysilicon in accordance with the present invention. As shown in FIG. 3A, the method utilizes a 25 conventionally processed semiconductor wafer 300 that has a top surface 310. Surface 310, in turn, has a number of substantially-equal lower levels 312 and a number of substantially-equal upper levels 314 that lie above the lower levels 312.

As further shown in FIG. 3A, the method begins by depositing a layer of polysilicon 320 on surface 310. Polysilicon layer 320 is conformally deposited and, as a result, also has a top surface that has a number of substantially-equal lower levels 322 and a number of substantially-equal upper levels 324 that lie above the lower levels 322.

5 Next, polysilicon layer 320 is conventionally doped. (Alternately, a doped layer of polysilicon can be formed in lieu of separate deposition and doping steps.) Following this, a layer of sacrificial oxide 330 is formed on polysilicon layer 320. Oxide layer 330 is also conformally 10 formed and, like polysilicon layer 320, has a top surface that has a number of substantially-equal lower levels and a number of substantially-equal upper levels that lie above the lower levels.

15 After this, as shown in FIG. 3B, oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished until oxide layer 330 is substantially, completely removed from the surface of polysilicon layer 320 to form a planarized layer of polysilicon 340. Once planarized polysilicon layer 340 has been formed, a mask (not shown) is formed and patterned on planarized polysilicon layer 340.

20 Next, planarized polysilicon layer 340 is etched to form a number of structures, such as local interconnect lines, that are electrically connected to individual devices on wafer 300. (The locations where the structures make electrical contacts with the individual devices of wafer 300 are prepared before polysilicon layer 320 is deposited, and are assumed to be a part of wafer 300.)

25 Alternately, after the planarization step, one or more additional layers of material, such as materials which lower the resistance of polysilicon, can be formed over layer 340. The mask is then formed and patterned on the additional layers of material which are then etched along with planarized polysilicon layer 340 to form the structures (e.g.,

local interconnect lines). Either way, once the structures have been formed, the method continues with conventional back-end processing steps.

When the structures are formed, the structures are specified to

5 have a thickness over the upper levels 314 that ranges from a minimum thickness to a maximum thickness. To achieve this result, polysilicon layer 320 is deposited to have a thickness such that lower level 322 is above upper level 314 by an amount which is at least as great as the minimum specified thickness of the resulting structures.

10 For example, if the minimum allowable thickness of the resulting structures over upper levels 314 is X (see FIG. 3B), then polysilicon layer 320 must be deposited so that lower level 322 is above upper level 314 by a value that is equal to or greater than the distance X (see FIG. 3A). (If the polishing is timed using experimentally derived values, then

15 polysilicon layer 320 is deposited so that lower level 322 is above upper level 314 by more than the distance X. This allows polysilicon layer 320 to be slightly over etched to insure that oxide layer 330 has been removed while still meeting the minimum requirements for the thickness of the resulting structures.)

20 In addition, oxide layer 330 is formed to have a thickness such that the combined thickness of polysilicon layer 320 and oxide layer 330 is approximately 2x-3x the required final thickness of the polysilicon layer. (Thicker layers of oxide can be used, but to no apparent advantage.)

25 Oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished with a slurry that ideally has a selectivity of 1:1 (removes oxide layer 330 at the same rate as polysilicon layer 320). In the present invention, slurries that fall within a range of approximately 0.9-1.1:1 can also be used. This approximate range is a critical range in

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that slurries that fall well outside of this range produce unacceptable dishing. (Slurries with a selectivity of 1.1:1 are commercially available.)

Although described with respect to polysilicon and oxide, materials other than oxide can alternately be used as a sacrificial

5 material if the material can be removed with a slurry that has a selectivity in the range of 0.9-1.1:1. In addition, the present invention applies to other thin films that can not be planarized using chemical-mechanical polishing. In this case, the other thin-film is combined with a material that can be removed with a slurry that has a selectivity in the

10 range of 0.9-1.1:1.

It should be understood that various alternatives to the embodiment of the invention described herein may be employed in practicing the invention. Thus, it is intended that the following claims define the scope of the invention and that methods and structures

15 within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:
 - 5 forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level
 - 10 that lies above the first lower level;
 - 15 forming a layer of second material on the top surface of the layer of second material; and
 - 15 chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of second material is all removed from the layer of first material to form the planarized layer of material.
- 20 2. The method of claim 1 wherein the first lower level lies above the wafer upper level.
- 25 3. The method of claim 2 and further comprising the step of etching the planarized layer of material to form a structure.
- 25 4. The method of claim 3 wherein the structure has a thickness that ranges from a minimum thickness to a maximum thickness over the wafer upper level.

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5. The method of claim 4 wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the minimum thickness.

5 6. The method of claim 1 wherein the first material is polysilicon.

10 7. The method of claim 1 wherein the second material is oxide.

10 8. The method of claim 1 wherein the structure is a local interconnect line.

15 9. The method of claim 1 wherein the first and second layers of material are chemically-mechanically polished with a slurry that has a selectivity that falls within an approximate range of 0.9-1.1:1.

15 10. The method of claim 2 and further comprising the step of forming a layer of third material on the planarized layer of material.

20 11. The method of claim 10 and further comprising the step of etching the layer of third material and the planarized layer of material to form a structure.

25 12. The method of claim 11 wherein the structure has a thickness that ranges from a minimum thickness to a maximum thickness over the wafer upper level.

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13. The method of claim 12 wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the minimum thickness.

5 14. The method of claim 1 and further comprising the step of doping the layer of first material prior to forming the layer of second material.

10 15. The method of claim 1 wherein the layer of first material is doped polysilicon.

16. The method of claim 3 wherein the layer of first material makes an electrical contact with a device on the wafer.

15 17. The method of claim 1 wherein the layer of second material is approximately two to three times as thick as the layer of first material.

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ABSTRACT

A layer of required material, such as polysilicon, is planarized by first forming a sacrificial layer of material, such as an oxide, on the layer of required material. The combined layers of required and sacrificial materials are then planarized using chemical-mechanical polishing until the sacrificial material has been substantially, completely removed.

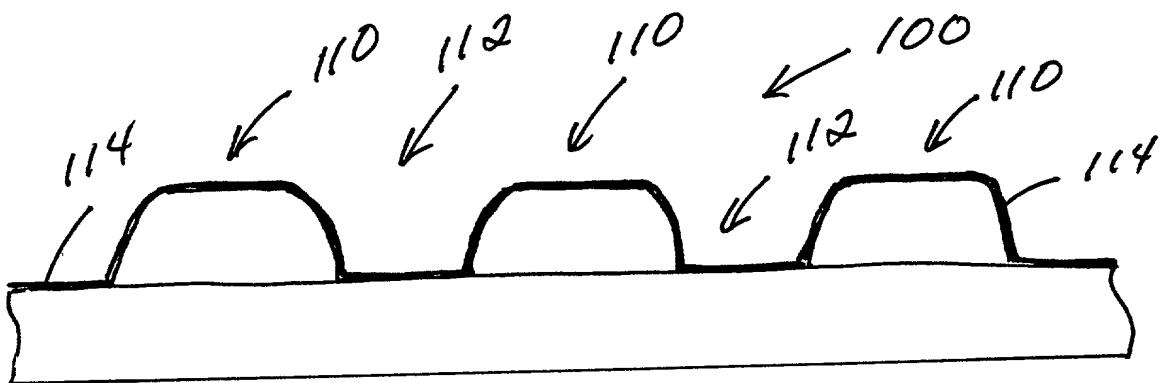


FIG. 1
(PRIOR ART)

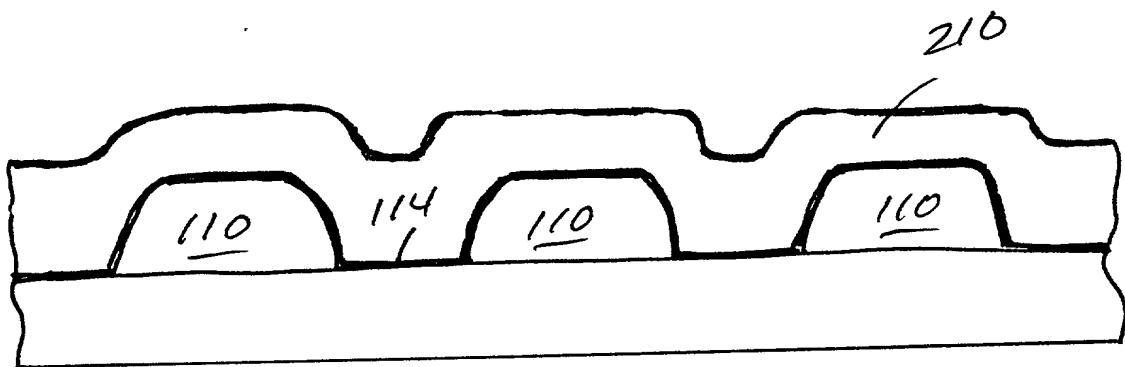


FIG. 2A
(PRIOR ART)

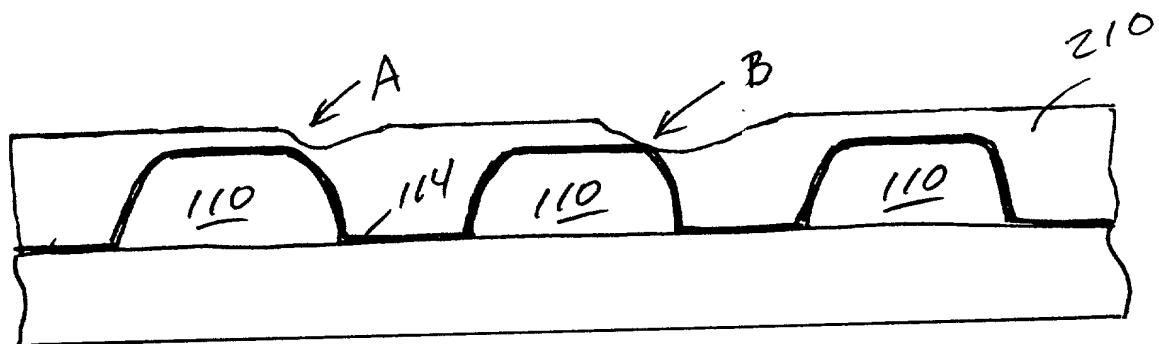


FIG. 2B
(PRIOR ART)

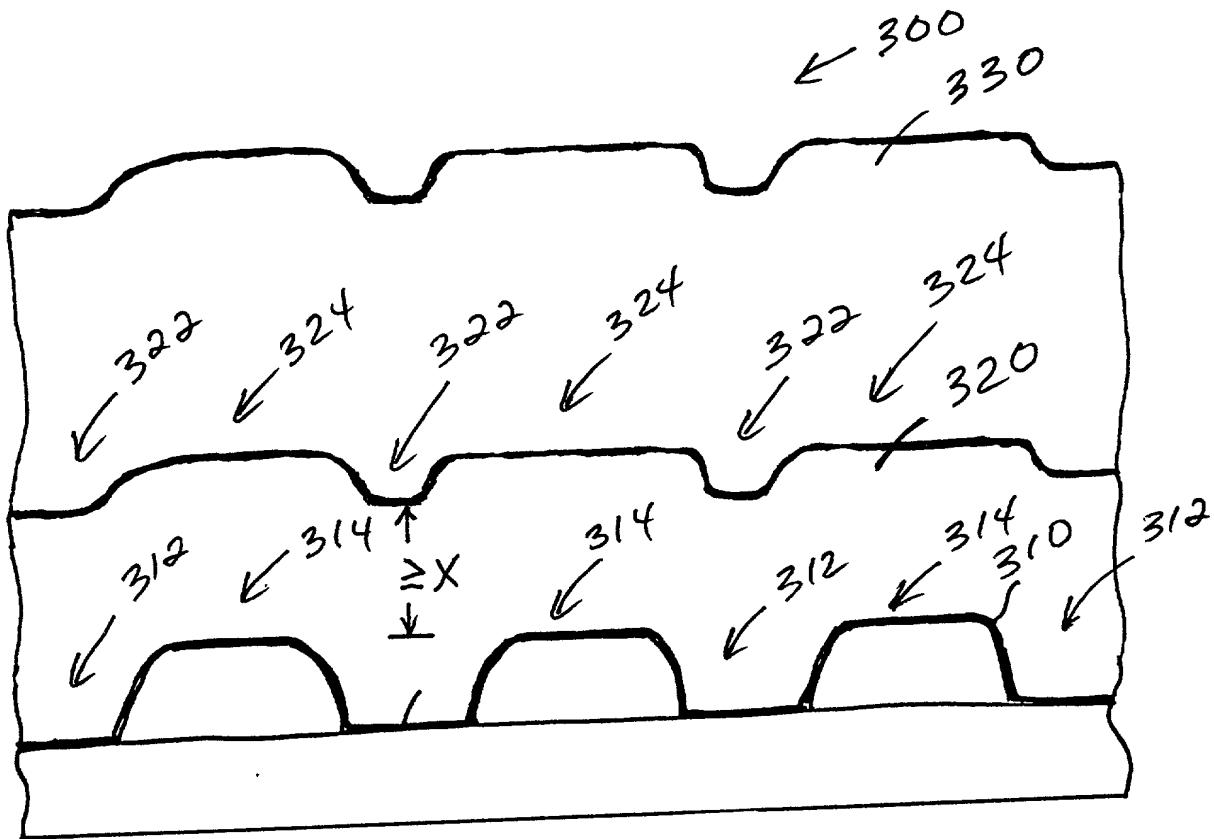


FIG. 3A

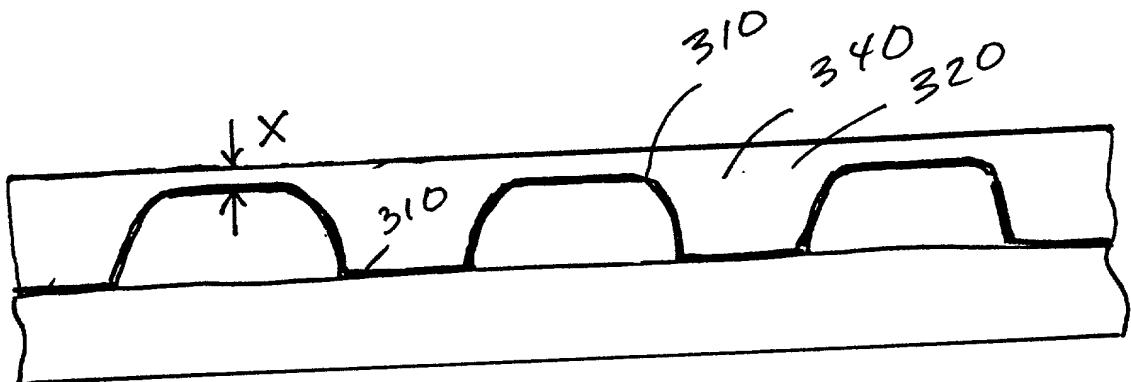


FIG. 3B

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR PLANARIZING A THIN FILM

the specification of which (check one) X is attached hereto or was filed on as Application No. and was amended on (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)	Priority Claimed	
	Yes	No

Number	Country	Day/Month/Year Filed		
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I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) below.

Application Number	Filing Date
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Application Number	Filing Date
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I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status: Patented, Pending, Abandoned
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Application Number	Filing Date	Status: Patented, Pending, Abandoned
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor DAVID W. CARLSON

Inventor's signature *David W. Carlson*

Date

9/26/02

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